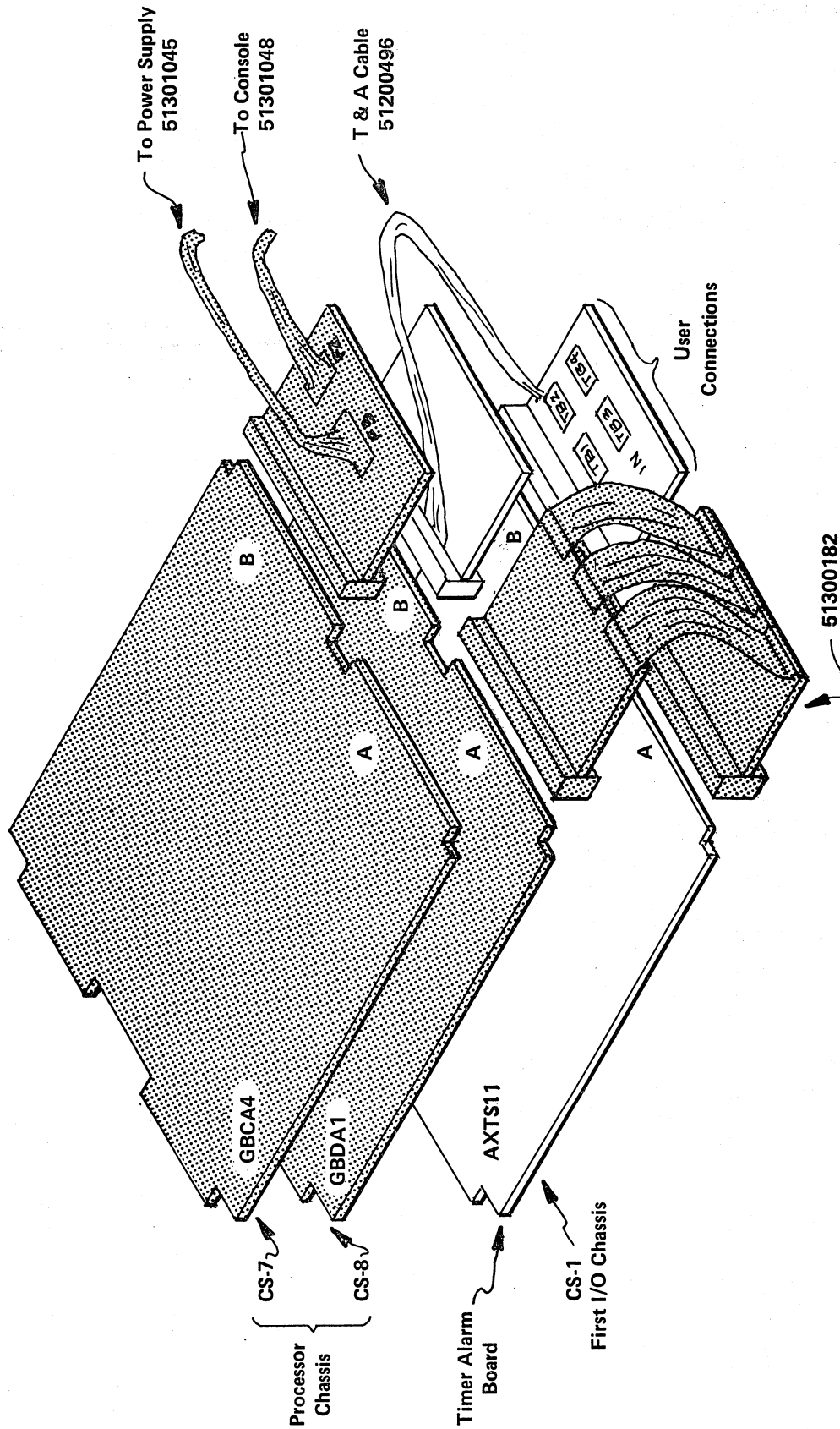

TABLE OF CONTENTS

1. INTRODUCTION	1
2. PRECAUTIONS	1
3. OPTIONS	1
3.1 Switch Options	1
3.2 Clip Options	1
4. REFERENCES	3
5. COMPONENT LOCATIONS	3
6. TEST EQUIPMENT AND MATERIALS	3
7. PREVENTIVE MAINTENANCE	3
8. PERFORMANCE TESTS	3
9. ASSEMBLY DISASSEMBLY	5
10. ADJUSTMENTS	5
11. TROUBLESHOOTING	5
11.1 Digital Outputs	5
11.2 Digital Inputs	5
11.3 Two kHz Clock	5
11.4 Alarms	8
12. PARTS	8



Note: Numbers Refer to Honeywell Wire Lists

Fig. 1 Timer Alarm Package Interconnections

TIMER AND ALARM PACKAGE MAINTENANCE INFORMATION

1. INTRODUCTION

The Timer and Alarm Package is a single printed wire assembly board (AXTS11) and interconnecting cables (see Fig. 1). It is a GENIE[®] Bus device which provides relay outputs from important signals in the Central Processor Unit (CPU). The TAP also provides processor interrupts from a precision timer, digital inputs and outputs and two remote control lines. Specifically it contains:

- Five alarm output relays
- One master alarm
- A 2 kHz ($\pm .01\%$) timer
- Eight digital output relays
- Four to eight digital input points
- Two CPU remote control lines*
- Two CPU status monitor inputs*
- One or two** general purpose relays.

All of the alarms plus up to two external alarm signals may (by jumper clip option) be combined into a master hardware alarm. The precision timer can be turned on or off by software. It requests an interrupt every 500 microseconds and can have a DMT echo interrupt. The digital I/O circuits transfer data to or from bits 0-7 in the CPU's A-register. Digital input lines may be used to disable the CPU console or to initialize the CPU from remote switches. Digital input lines may also be used to tell if the stall alarm has been locked out or if interrupts have been locked out. TAP operation is explained in Honeywell publication ATAP11-T. Parts 3 and 11 of this publication shows many of the CPU interconnections.

2. PRECAUTIONS

Only logic level voltages are present on the Timer and Alarm board. Use normal precautions when handling the board:

- Power down before inserting/removing a board.

*Each of these signals take a digital input line.

**One relay is shared with an alarm driver.

- Avoid touching connector pins.
- When replacing a board, duplicate its switch and clip settings on the new one.

AAXTB1 terminal board connections should be made with power off. If this isn't possible, be careful with TB3 terminals 1-3 which could initialize the system or disable the console. These remote control lines are shown on 51300966 logic sheet 10.

3. OPTIONS

3.1 Switch Options

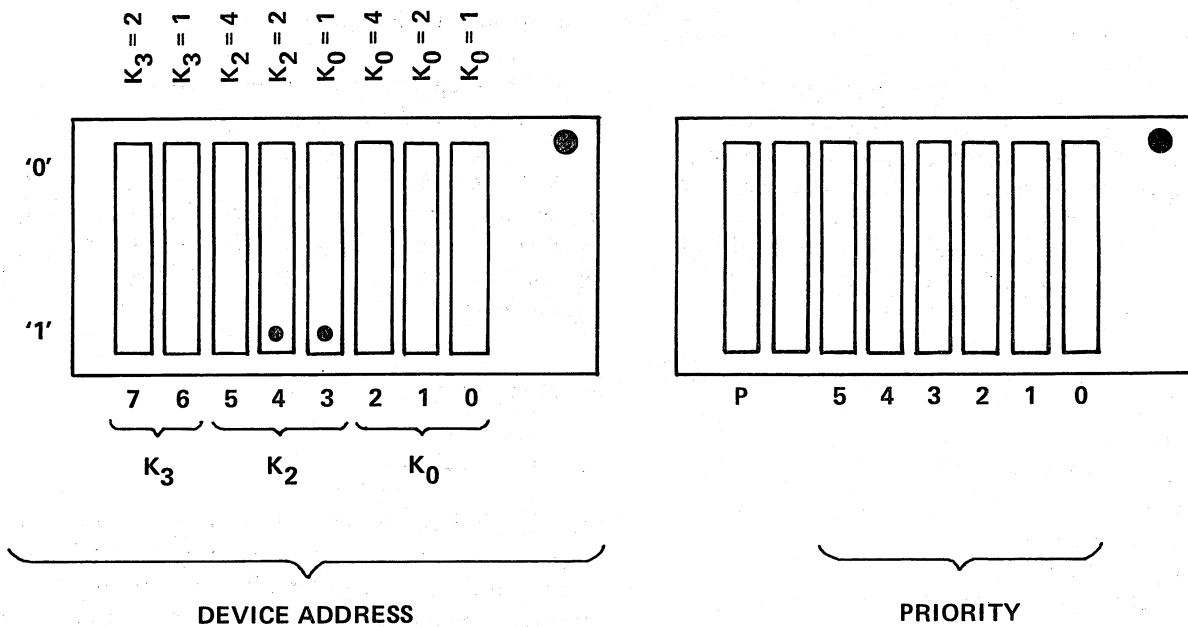
Fig. 2 shows the AXTS11 address and priority switches. They are set to factory assigned values and should not need to be changed. The K3=4 bit is always assumed to be a '1' if an even number of address switches are set. A typical address might be 4300_g in which case the address switches would be set to 030_g.

Priority switch settings determine which GENIE Bus controller is serviced first in case more than one device requests interrupt service at the same time. No two device controllers may have the same priority. TAP interrupts are used by the 2 kHz precision timer.

3.2 Clip Options

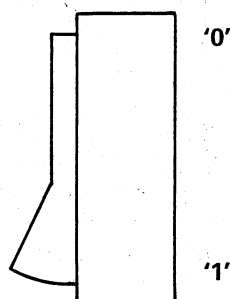
Clip options are diagrammed on logic sheet 0.5. SP3-SP7 are inputs to the master hardware alarm. Two external inputs may also be brought through TB4-4 or 5 to the master alarm. All or none of the inputs may be used. External inputs to the master alarm go low in the alarm state.

SP2 and 13 switch the memory alarm relay from internal to external use; see Fig. 3 or logic sheet 9. Clips SP8 and 9 tie the remote control functions "console disable" and "remote initialize" on with digital input lines 7 and 6 respectively. Clips SP10 and 11 switch digital inputs 4 and 5 from terminal board inputs to status monitors (stall alarm locked out and interrupts locked out). See logic sheet 10 and Fig. 4 regarding clips SP8-11. Clips SP1 and SP12 should always connect K4 to the external lines for use as a general purpose relay.



DEVICE PRIORITY

Priority (High to Low)	Switches						
		5	4	3	2	1	0
H 01 (33 ₈)		0	1	1	0	1	1
02 (35 ₈)		0	1	1	1	0	1
03 (36 ₈)		0	1	1	1	1	0
04 (37 ₈)		0	1	1	1	1	1
05 (53 ₈)		1	0	1	0	1	1
06 (55 ₈)		1	0	1	1	0	1
07 (56 ₈)		1	0	1	1	1	0
08 (57 ₈)		1	0	1	1	1	1
09 (63 ₈)		1	1	0	0	1	1
10 (65 ₈)		1	1	0	1	0	1
11 (66 ₈)		1	1	0	1	1	0
12 (67 ₈)		1	1	0	1	1	1
13 (73 ₈)		1	1	1	0	1	1
14 (75 ₈)		1	1	1	1	0	1
15 (76 ₈)		1	1	1	1	1	0
L 16 (77 ₈)		1	1	1	1	1	1



Side View
'0' Shown

Fig. 2 Switch Options

4. REFERENCES

The following publications are either useful or necessary to understand and maintain the Timer Alarm Package:

Timer and Alarm Logic Drawing	51300966
Theory of Operation - TAP	ATAP11-T
CPU Console Logic	51301069
Power System Logic	51300824
GENIE Controller Logic	51300542
Memory Bus Controller Logic	51301111
Instruction Test Program	51191048

5. COMPONENT LOCATIONS

Fig. 1 shows major parts of the TAP subsystem. The AXTS11 board must be placed in card slot 1 of the first I/O chassis. The Timer and Alarm cable and terminal board assembly goes between connector field B of processor card slot 8 and card slot 1 of the 1'st I/O chassis.

User connections to the terminal board assembly are summarized on the 51300966 logic sheets 12 and 13. Clip positions are marked on the AXTS11 board and shown by a drawing on logic sheet 0.5.

6. TEST EQUIPMENT AND MATERIALS

Normal electronic test equipment such as a good oscilloscope and multimeter will be needed for troubleshooting beyond the board replacement level.

A Timer Alarm Test Plug is needed to run the turnaround part of the test described in part 8. Performance Tests. One additional alarm line (red/blue error) can be tested if a PX4000GDEBA1 GENIE Device Emulator board (and a test plug) is available.

The test plug is substituted for the T & A cable shown in Fig. 1. Test plugs are not available from Honeywell, but a standard T & A cable assembly (4DP3AAZTA1) may be made into a test plug by wiring it as follows:

<u>Jumpers</u>			
<u>From</u>	<u>To</u>	<u>From</u>	<u>To</u>
TB1-1	TB4-2	TB2-4	TB3-3
TB1-3	TB4-1	TB2-5	TB3-1
TB1-4	TB3-10	TB2-6	TB3-2
TB1-6	TB4-1	TB2-10	TB3-4
TB1-7	TB3-9	TB4-10	TB3-5
TB1-9	TB3-8	TB4-8	TB3-6
TB1-10	TB3-7	TB4-7	TB3-5
TB2-2	TB3-8		

Then cut artwork run between B39 and B40 on the terminal board assembly card (11th and 12th pads from top right side at the connector). Solder a jumper wire to pin B39 and connect the other end to TB4-9 (see Fig. 5).

7. PREVENTIVE MAINTENANCE

AXTS11. There aren't any adjustments on the TAP and all relays are sealed, so no preventive maintenance is needed.

AAXTB1. Check screw terminals for tightness yearly or whenever making any wiring changes.

System. Related power system adjustments may affect the TAP; see part 10. Adjustments. The test programs described in part 8. Performance Tests, should be run after installation, after repairs to the TAP or when the TAP has not been in use for extended periods.

8. PERFORMANCE TESTS

The Timer Alarm Package is tested using Honeywell Instruction test 51191048. A test plug (see 6 Test Equipment) is used to route output signals back through TAP input paths (see Fig. 5). The standard 60 Hz clock is compared with the TAP's 2 kHz clock, so interrupts must not be locked out during the test. If a GDEBA1 GENIE emulator board is present, the program will test the blue memory alarm line. Part 2 of the test program write-up tells how to use it and part 3 describes the Timer Alarm Package test. If a test plug isn't available, the program will test only the 2 kHz clock and skip all turnaround tests.

Before starting the test, refer to 51300966 logic sheet 0.5 and set TAP clips as follows:

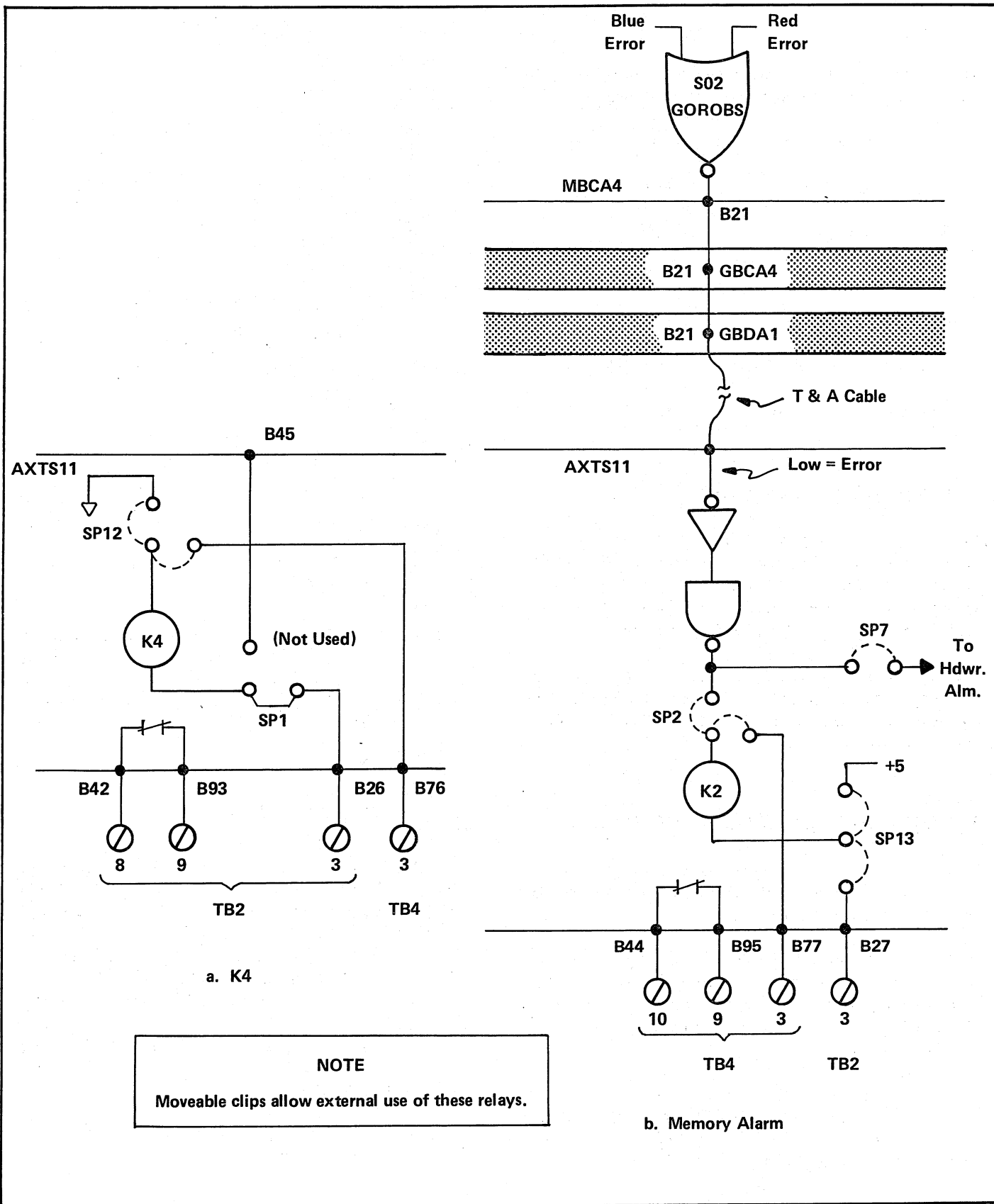


Fig. 3 Internal/External Alarm Switching

<u>Clip</u>	<u>Signal</u>
SP1	External input to K4
SP2	RD/BL to K2
SP3,4,5,7	Remove clips
SP6	In - (PMCE to HDWR alarm).
SP8	AUXCE to X0BB07
SP9	Store
SP10	DIICA2 to X0BB05
SP11	DIICA2 to X0BB04
SP12	External to K4
SP13	Internal +5 V to K2

Replace the standard T & A cable with a test cable. Run the test program with manual intervention tests, interrupts and the stall alarm enabled and with the keyswitch in the console enable position. You may need to re-enable interrupts and the stall alarm during this test if programmed stalls etc. cause them to be reset.

9. ASSEMBLY DISASSEMBLY

The Timer Alarm Package contains only a plug-in board and an interconnecting cable. It must go into card slot 1 of the first I/O chassis. Cable 4DP3AAZTA1 goes on the backpanel between field B of the AXTS11 board and the GBDA1 board (see Fig. 1). User connections go to a terminal board which is part of the timer and alarm cable.

10. ADJUSTMENTS

There aren't any adjustments on the TAP board. An under-voltage adjustment and a power interruption adjustment in the power supply will affect the power fail alarm. Honeywell publication ACPU1PS-M on the TDC 4500 power subsystem tells how to make these adjustments.

The stall alarm timer may be set for approximately 1, 2, or 4 seconds (or disabled) by clip option. You will find it on the GBCA4 GENIE Bus controller board.

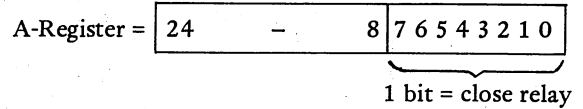
11. TROUBLESHOOTING

Many areas of the TAP go through cables and backpanel artwork to monitor or control some CPU function. Figures in this maintenance publication are detailed to show the signal flow. Notes on these diagrams tell you what voltage level causes an alarm or what voltage to expect when input terminals are shorted. Many troubles could easily be in one of the connections rather than the TAP board. Theory publication ATAP11-T tells more about each area. The test program described in part 8. Performance Tests, checks most of the TAP circuits. Here is some information that may help you check each TAP area. Numbers in () refer to 51300966 logic.

11.1 Digital Outputs

These are normally open relay contacts that close when you place "1" bits in the A register and execute an OUT command addressed to the TAP (sh. 8).

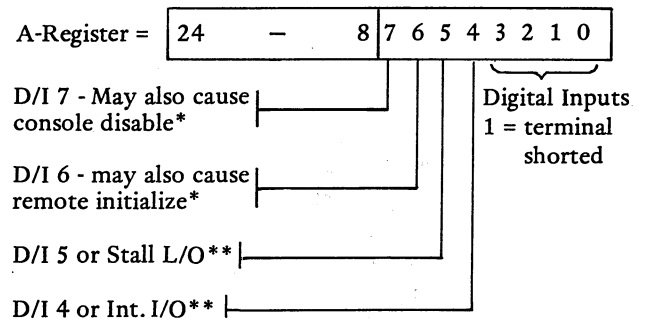
OUT - 2504DD0D
DDD = TAP address



11.2 Digital Inputs

An IN command addressed to the TAP will bring a "1" bit into the CPU's A register when digital input terminals are shorted (sh. 10). This is always true with bits 0-3 and bits 6 and 7. Bits 6 and 7 may (by clip option) also remotely control the CPU as shown in Fig. 4a. Bits 4 and 5 may work just like 0-3 or (by clip option) either may monitor a CPU status (see Fig. 4b).

IN - 2505DD0D



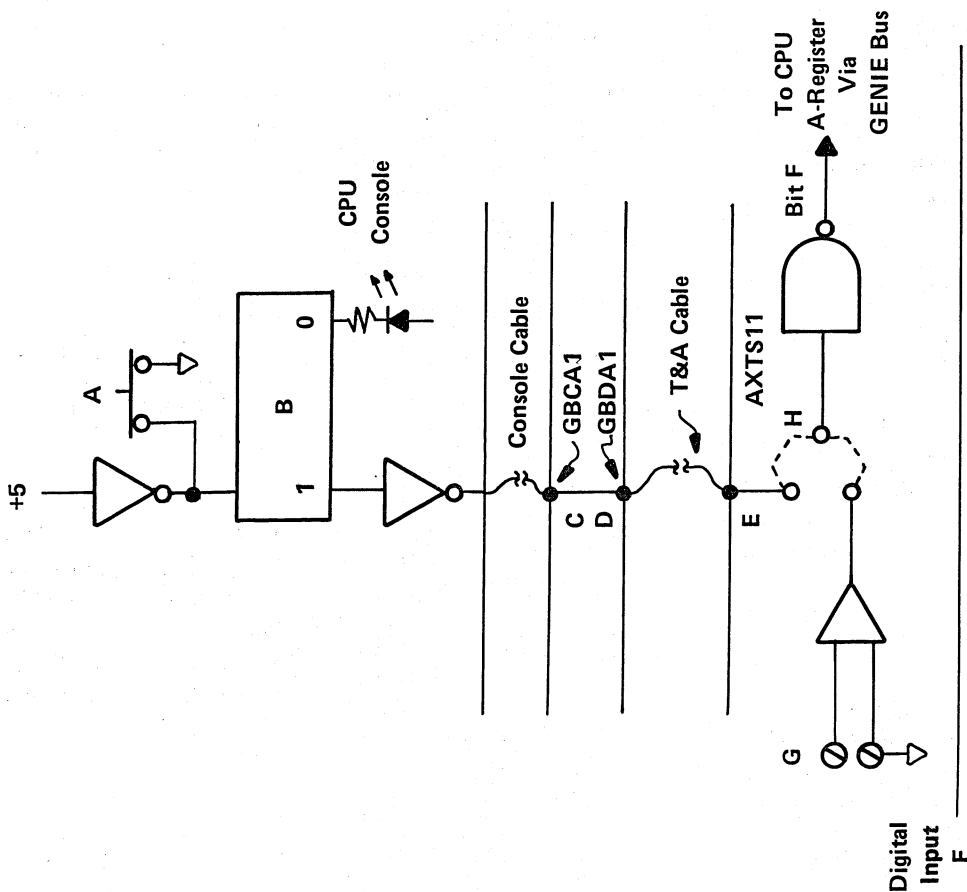
11.3 Two kHz Clock

The clock is initialized off. If you execute an operate (OPR) command with S' bits = 1, it should start. An OPR with S'=0 turns it off. The clock requests an interrupt every 500 microseconds (sh. 7). Interrupts can be masked by the AIM command.

When the clock has been enabled, you should find a 174 nanosecond pulse period leaving the oscillator on logic sh. 7 and a 2.78 microsecond pulse period leaving F1TLS8. The other counters work a little differently than you might suspect, but this is explained in theory publication ATAP11-T. The 2 kHz pulse period from F1TSA requests interrupts every 500 microseconds.

*A register bit will be a binary 0 when remote control function (if used) is asserted.

**A register bit = 0 when monitored function (if used) is locked out.



Digital Inputs 4 & 5 (See Table)

A	B	C	D	E	F	H
Input	TB3	Clip	Pin	Pin	Pin	Destination
6	3 & 2	SP9	B83	B33	B83	N1CRST On GBCA4
7	1 & 2	SP8	B55	B55	B55	R1AXCE Via Console Cable

a. Digital Inputs 6 and 7 and/or Remote Control

A	B	C	D	E	F	G	H
Switch	F/F	Pin	Pin	Pin	Input	TB3	Clip
Int. L/O	F1ILOF	B37	B36	B37	4	6 & 5	SP-11
Stall L/O	F1STLO	B38	B38	B38	5	4 & 5	SP-10

b. Digital Inputs 4 and 5 or Status Monitors

(open input at Point B causes low level at Point H)

Fig. 4 Digital Inputs 4 - 7

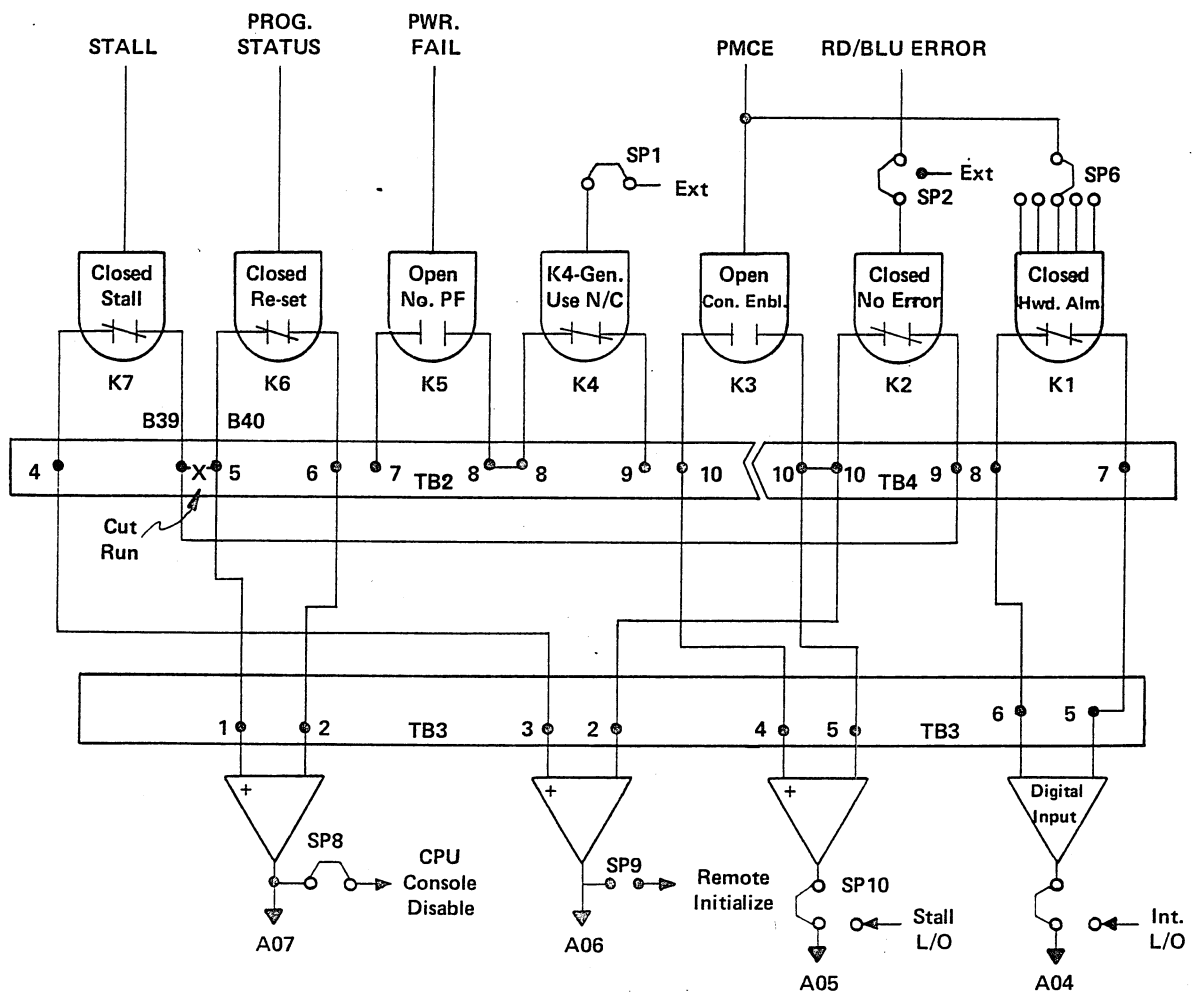
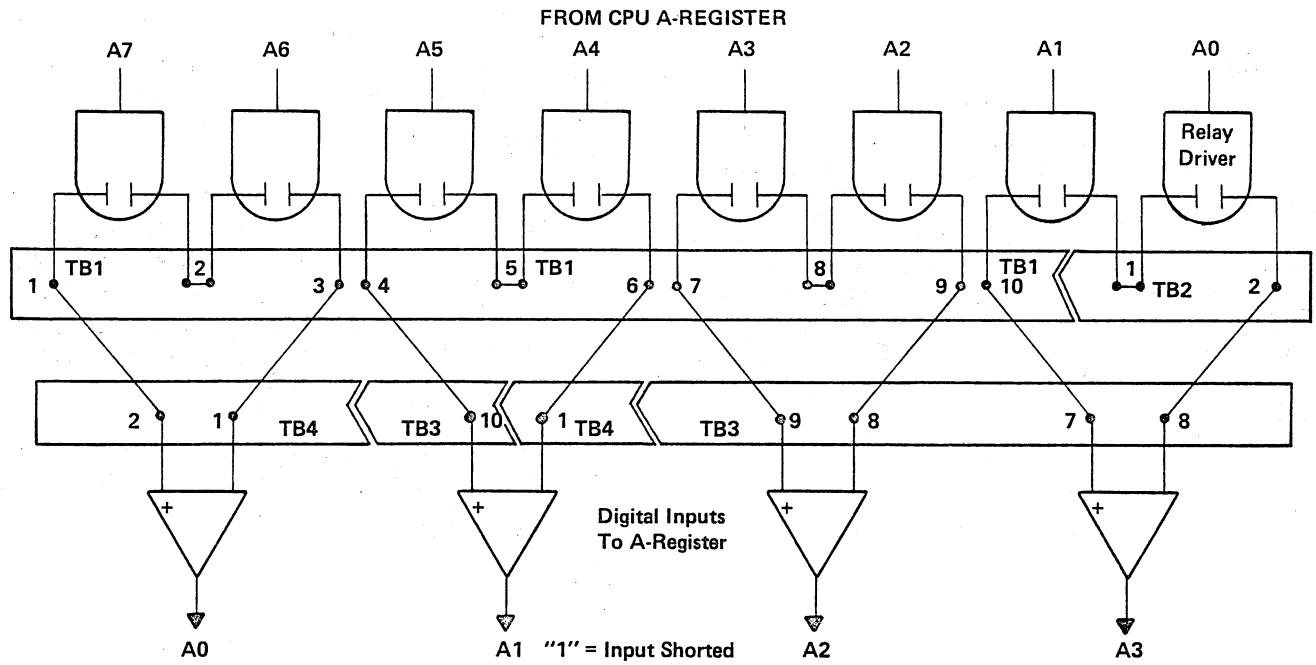


Fig. 5 Test Cable Paths

11.4 Alarms

Alarm relay contacts are open when the coil is energized (sh. 9). Some will normally be energized; others won't (see comments on Fig. 5). The master hardware alarm relay contacts are normally held open but close on alarm (a low input to G1HDWR). Some of the alarms can be easily tested. You can switch the programmed status relay on or off with software. A set alarm command (SALM) 25014000 should energize K6 and a reset alarm (RALM) 25024000 should release it. PMCE alarm relay K3 should energize when the keyswitch enables the console. K3 should release (close its contacts) when the keyswitch disables the console. K2 can be used for memory alarm service or as a general purpose relay by moving jumper clips.

Figs. 6 and 7 illustrate the alarm signal flow. Also see Fig. 3b where the memory alarm is illustrated.

12. PARTS

Honeywell PL drawing 4DP3AAXTS11 lists all replaceable parts for the AXTS11 board. The B field backpanel terminal board and cable parts are listed on PL drawing 4DP3AAXTB11. Refer to Fig. 1 for wire list numbers. Numbers for the console cable, A-field backpanel cable and power supply cables are also shown on Fig. 1, but they are not part of the Timer Alarm Package.

Test Plug. — The Timer Alarm Test Plug is a standard 4DP3AAXTB11 cable wired as shown in part 6 of this publication. publi

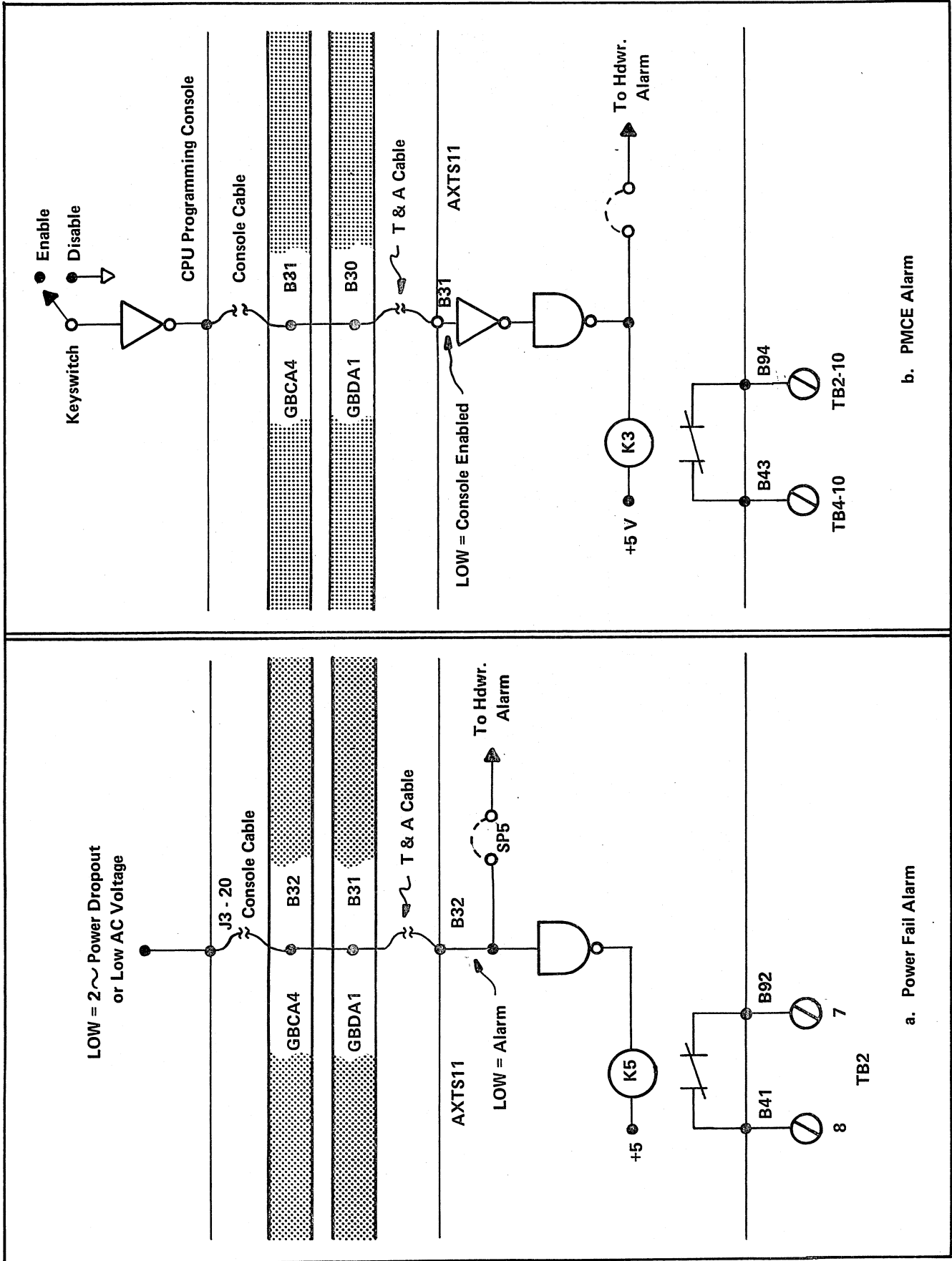


Fig. 7 Power Fail and Console Enabled Alarm

READER COMMENTS

In order to improve future editions of this and other publications, Honeywell's Process Control Division/Phoenix solicits your comments. You may direct them to the writer through this form, by letter, or telephone. His address and phone number are provided below. Some of the factors contributing to the usefulness of this publication are listed below. Please explain any "no" responses in the COMMENTS section.

Writer: Bill Damours /tg/gg (602) 943-2341 Ext. 436
 Honeywell Inc.
 Publications - 130 HVN 364-1 436
 2222 W. Peoria Ave.
 Phoenix, Arizona 85029

- Publication No. ATAP11-M
- How is this publication used:

Familiarization <input type="checkbox"/>	Reference <input type="checkbox"/>
Training <input type="checkbox"/>	Maintenance <input type="checkbox"/>
Other (Explain) _____	

- | | YES | NO |
|--|--------------------------|--------------------------|
| • Does this publication meet your requirements | <input type="checkbox"/> | <input type="checkbox"/> |
| • Is the material: | | |
| 1) Presented in clear text | <input type="checkbox"/> | <input type="checkbox"/> |
| 2) Conveniently organized | <input type="checkbox"/> | <input type="checkbox"/> |
| 3) Adequately detailed | <input type="checkbox"/> | <input type="checkbox"/> |
| 4) Adequately illustrated | <input type="checkbox"/> | <input type="checkbox"/> |
| 5) Presented at appropriate technical level | <input type="checkbox"/> | <input type="checkbox"/> |
| 6) Technically accurate | <input type="checkbox"/> | <input type="checkbox"/> |

- Please provide specific text references (page number, line, etc.) with your comments.

NAME _____ DATE _____
 TITLE _____
 COMPANY NAME _____
 AND ADDRESS _____

COMMENTS:

Staple

Communications concerning technical publications should be directed to:

Technical Publications - 130
Process Control Division/Phoenix
Honeywell Inc.
2222 West Peoria Avenue
Phoenix, Arizona 85029

Fold

Fold

FIRST CLASS
Permit No. 4091
Phoenix, Arizona

BUSINESS REPLY MAIL

NO POSTAGE NECESSARY IF MAILED IN THE UNITED STATES

POSTAGE WILL BE PAID BY...

PROCESS CONTROL DIVISION/PHOENIX
HONEYWELL INC.
2222 West Peoria Avenue
Phoenix, Arizona 85029



Cut Along Line

Attention: Manager, Marketing Communications - 140

Fold

Fold